CS 59300ACA: Advanced Computer Architecture

CS593 Graduate level (MS and Ph.D)

Course title: Advanced Computer Architecture

Course Description:
This course covers the concepts and techniques for conducting research and industry career related to computer architecture. The course explores the topics of computer architecture at a higher and more abstract level than prior courses on computer organization. In this course, we will learn the essential techniques that are used in designing modern computer architectures from single/multi-processors to warehouse-scale computers. We will introduce both general techniques including, technology trends, memory hierarchy, instruction-level parallelism, data-level parallelism, thread-level parallelism, cache coherence/consistency; and the design principles and examples of the domain-specific architectures.

The students taking the course are expected to finish written homeworks, attend the mid-term exams and a final exam. The course also comes with a number of projects on architecture simulation and quantitative performance evaluation.

Administrative Information:
Name: Xuehai Qian
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TAs: TBD
Time & Location: TTh 9:00a-10:15a LWSN B134
Course website: TBD

Course Materials:
1. (Required) John L. Hennessy and David A. Patterson. "*Computer Architecture. A Quantitative Approach*". Sixth Edition. Morgan Kaufmann, 2017
2. (Optional) Dubois, Annavaram and Stenström: "*Parallel Computer Organization and Design*" Cam-bridge University Press, 2012

3. (Optional) John Cheng, Max Grossman, Ty McKercher: "*Professional CUDA C Programming*". John Wiley & Sons, Inc, 2014

Prerequisites:

CS250. Computer Architecture

Tentative Course Schedule:

Date	**Topic**	**Assign**	**Due**
8/23	Fundamentals of quantitative design (I)		
8/25	Fundamentals of quantitative design (II)		
8/30	Instruction set principle	HW1 assigned 8/30	HW1 due 9/6
9/1	Memory hierarchy basics (I)	PA1 assigned 9/1	PA1 due 9/12
9/6	Memory hierarchy basics (II)		
9/8	Memory hierarchy design (I)		
9/13	Memory hierarchy design (II)	HW2 assigned 9/13	HW2 due 9/20
9/15	Pipelining: basic and intermediate (I)	PA2 assigned 9/15	PA2 due 9/26
9/20	Pipelining: basic and intermediate (II)		
9/22	Instruction-level parallelism (I)		
9/27	**Mid-term exam 1**	**scope: materials from 8/23 — 9/20**	
9/29	Instruction-level parallelism (II)	HW3 assigned 9/29	HW3 due 10/6
10/4	Data-level parallelism: vector and SIMD	PA3 assigned 10/4	PA3 due 10/12
10/6	Data-level parallelism: GPU (I)		
10/13	Data-level parallelism: GPU (II)	HW4 assigned 10/13	HW4 due 10/20
10/18	**Project proposal presentation**	Proposal due 10/24	
10/20	Data-level parallelism: GPU (III)	PA4 assigned 10/20	PA4 due 10/31
10/25	**Mid-term exam 2**	**scope: materials from 9/22 — 10/20**	
10/27	Thread level parallelism (I)		
11/1	Thread level parallelism (II)		
11/3	Parallel architecture (I)		

11/8	Parallel architecture (II)		
11/10	Parallel architecture (III)	HW5 assigned 11/10	HW5 due 11/17
11/15	Interconnection networks	PA5 assigned 11/15	PA5 due 11/22
11/17	Domain-specific architectures: Graph		
11/22	Domain-specific architectures: ML (I)		
11/29	Domain-specific architectures: ML (II)		
12/1	Project presentation (I)		
12/6	Project presentation (II)		
12/10	Project presentation (III)		
TBD	Final exam	**scope: all lectures**	

Grading Policy:
There will be six homeworks (HW), five project assignments (PA), one final project (proposal and final report), two mid-term exams, and one final exam.

- Homeworks (5×5%): 25%
- Project assignments (5*4%): 20%
- Project proposal and presentation: 3%
- Final report and presentation: 7%
- Mid-term 1: 10%
- Mid-term 2: 10%
- Final exam: 25%

Project: students are encouraged to work as teams of two or three.
Project proposal and report template: will be provided
Late submission policy: All deadlines are firm unless notified in advance. Late submissions can be only accepted within next 48 hours of the deadline but will result in a straight 25% off.

Academic Integrity:
This course defaults to Purdue standards on intellectual integrity and academic conduct. Therefore, students are responsible for reading the following pages and comply with them throughout this course.

- https://spaf.cerias.purdue.edu/integrity.html

- https://spaf.cerias.purdue.edu/cpolicy.html

Statement for Students with Disabilities:
Purdue recognizes that inclusion and access are a University-wide responsibility. Active participation by faculty, students and DRC staff are key to creating accessible experiences. Please consult this website for detailed information: https://www.purdue.edu/drc/faculty/index.php